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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/241,177	02/01/1999	SALMAN AKRAM	3638US-(98-0	8330

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EXAMINER	
NOVACEK, CHRISTY L	
ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 03/19/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/241,177	AKRAM ET AL.	
	Examiner	Art Unit	
	Christy L. Novacek	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 January 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *32-39 and 44-51* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *32-39 and 44-51* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 January 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

This Office Action is in response to the communications filed January 8, 2003 and October 8, 2002.

Drawings

The corrected drawings were received on January 8, 2003. These drawings are acceptable.

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 32-37, 39, 44-49 and 51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chan et al. (US 5,998,860, previously cited) in view of Lin et al. (US 5,239,198, cited in IDS).

In reference to claims 32 and 44, Chan discloses a plurality of semiconductor dice (50) each having an active surface and a plurality of bond pads (120). A planar substrate (70) has opposing first and second sides (92, 94) and at least three elongate through-slots (86) extending from the first side to the second side. A pattern of conduits (118) (inherently electrical conductors) is formed on each side of the substrate and is connected to terminal contacts (82) that are adjacent to the through-slots on the substrate. The terminal contacts connect the bond pads of the dice to the conduits which, in turn, connect to an input/output connector (104). The active surfaces of some of the dice are attached to the first side of the substrate and the bond pads of the dice are aligned with alternate through-slots for access from the second side of the

substrate. The active surfaces of some of the other dice are attached to the second side of the substrate and the bond pads of these dice are also aligned with alternate through-slots for access from the first side of the substrate. The bond pads of the dice are wire-bonded to the terminal contacts adjacent the through-slots. See Fig. 1 and 2 and col. 4, ln. 37-63.

Chan does not specifically disclose that the conductor patterns on each side of the substrate are connected by vias in the substrate. However, Chan discloses that his invention is specifically directed to a double-sided single inline memory module (SIMM) (Title; claims 1-16). Inherently, a SIMM package has all of the dice within the package electrically connected (please see the PC Guide Internet reference, enclosed herein). Chan discloses that the conductor patterns (118) on the substrate electrically connect the dice to one another (col. 4, ln. 60-63). Like Chan, Lin discloses a SIMM multi-chip module in which semiconductor dice are attached to opposite surfaces of a printed circuit board (Fig. 10). The semiconductor dice on the top surface of the circuit board of Lin are wire bonded to conductive traces on the top surface of the board and the semiconductor dice on the bottom surface of the circuit board are electrically connected to conductive traces on the bottom surface. Lin states that conductive traces on the top surface of the board are connected to traces on the bottom surface of the board by way of conductive through-holes (vias) within the board in order that the dice on both sides of the board can share power and ground traces (col. 3, ln. 40-53). At the time of the invention, it would have been obvious to one of ordinary skill in the art to connect the dice on both sides of the package to each other through conductive vias within the board because a SIMM conventionally has all of its dice electrically connected to one another and, as is taught by Lin, the dice on both sides of

the board usually share power and ground traces within the board so as to avoid needlessly duplicating the power and ground circuitry.

Chan discloses an input/output connector of tabs (104) formed on the edge of the substrate, which are used to mount the package vertically into a socket on a higher-level circuitry board (col. 4, ln. 58-61). Chan does not disclose forming a ball-grid array (BGA). Like Chan, Lin discloses the multi-chip module to have an input/output connector of tabs on upper and lower surfaces of the board to which the conductive traces on the upper and lower surfaces of the board are connected (Fig. 10; col. 45-65). Lin discloses attaching solder balls onto the input/output connector tabs located on the peripheral area of the board and subsequently using these solder balls to attach the multi-chip module to higher-level circuitry (col. 7, ln. 40-58). Lin states that by using solder balls to fortify the conventional SIMM socket connection, the solder balls provide a rigid support to securely attach the multi-chip module to the higher-level circuitry (col. 7, ln. 42-44, ln. 55-58). At the time of the invention, one of ordinary skill in the art would have found it obvious to form an array of solder balls on the peripheral area of the board because Lin teaches that the solder balls provide a more secure connection between the multi-chip module and the higher-level circuitry board than is achievable by using the socket connection alone.

In reference to claims 33 and 45, Chan discloses that the through-slots are made by forming an elongate stepped surface in the through-slots (Fig. 2-4).

In reference to claims 34 and 46, Chan discloses that the conductive connection terminals are formed on the elongate stepped surface (Fig. 3-4).

In reference to claims 35 and 47, Chan discloses that a glob-top material (90) is inserted into each through-slot to encapsulate the wires (Fig. 1; col. 5, ln. 49-59). This material is disclosed to be a resin. Inherently, the resin must be initially flowable in order to be capable of encapsulating the wires. The resin must also be hardenable, otherwise the encapsulant would be useless for protecting the wires from damage.

In reference to claims 36 and 48, Chan discloses a resin (inherently hardenable and polymeric – see attached Kirk-Othmer reference) material is inserted into each through-slot (Fig. 1; col. 5, ln. 49-59).

In reference to claims 37 and 49, as can been seen in Figure 1, Chan discloses that the glob-top material is inserted to extend outwardly between the edges of at least two die proximate each side of the through-slots.

In reference to claims 39 and 51, Chan discloses that the polymeric glob-top material is also used to encapsulate/seal the die (Fig. 1, 5; col. 6, ln. 54-58).

Claims 32, 38, 44, and 50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chiu (US 5,243,497, previously cited) in view of Lin et al. (US 5,239,198).

In reference to claims 32 and 44, Chiu discloses a plurality of semiconductor dice (32) each having an active surface and a plurality of bond pads (35). A planar substrate (31) made of a circuit board has opposing first and second sides and at least three elongate through-slots (33) extending from the first side to the second side. Chiu discloses that the dice are connected to a pattern of terminal contacts (34) on each side of the board and that these contacts are part of the circuitry on the circuit board. These contacts (inherently electrical conductors) are adjacent to the through-slots on the substrate (col. 2, ln. 2-9).

The active surfaces of some of the dice are attached to the first side of the substrate and the bond pads of the dice are aligned with alternate through-slots for access from the second side of the substrate. The active surfaces of some of the other dice are attached to the second side of the substrate and the bond pads of these dice are also aligned with alternate through-slots for access from the first side of the substrate. The bond pads of the dice are wire-bonded to the terminal contacts adjacent the through-slots. See Fig. 3-5 and col. 2, ln. 2-9 and ln. 33-47.

Chiu discloses that the contacts (34) are connected to vias that are connected with other layers of the circuit board (col. 2, ln. 8-11), but does not specifically disclose that the conductor patterns on each side of the substrate are connected to each other. Like Chiu, Lin discloses a multi-chip module in which semiconductor dice are attached to opposite sides of a printed circuit board (Abstract). Lin discloses that the dice on either side of the board are electrically connected to one another through conductive vias that are within the board. Lin states that the conductive vias allow the semiconductor dice on both sides of the board to share power and ground circuitry located within the board. At the time of the invention, it would have been obvious to one of ordinary skill in the art to connect the dice on both sides of the package to each other through conductive vias within the board because, as is taught by Lin, it is conventional to have the semiconductor dice on both sides of the board share power and ground circuitry within the board so as to avoid needlessly duplicating the power and ground circuitry.

Chiu does not disclose the circuit board (substrate) to have an input/output connector. However, the circuit board must inherently have some type of an input/output connector so that the semiconductor dice can be electrically accessed. Similarly, the input/output connector must also inherently be connected to the terminal contacts (34) in order to be electrically connected to

the dice. Lin discloses that a multi-chip module such as that of Chiu may be attached to higher-level circuitry either vertically or horizontally (Fig. 4, 9). In either case, the multi-chip module uses a ball-grid array located on the periphery of the board to securely attach the module to additional circuitry. At the time of the invention, it would have been obvious to one of ordinary skill in the art, to form the inherent input/output connector of Chiu such that it includes a ball-grid array on the periphery of the substrate because, as is shown by Lin, a ball-grid array can be used to attach a multi-chip module to higher-level circuitry whether the module is attached vertically or horizontally.

In reference to claims 38 and 50, Chiu discloses that the semiconductor dice is electrically tested following wire-bonding but prior to any wire encapsulation (col. 2, ln. 31-32).

Claims 35-37, 39, 47-49 and 51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chiu in view of Lin et al., as applied to claims 32 and 44 above, and further in view of Chan et al.

In reference to claims 35, 36, 47 and 48, Chiu discloses that a glob-top material (36) is inserted into each through-slot to encapsulate the wires, but does not disclose what type of encapsulant is used (Fig. 4; col. 2, ln. 31-32). However, encapsulants used to protect wires in an integrated circuit package typically comprise a flowable, hardenable polymeric material, such as a resin, as is disclosed by Chan (Fig. 1; col. 5, ln. 49-59). The encapsulant must be flowable so that the material can completely surround and seal the wires while also being hardenable so that it can protect the wires from breakage. At the time of the invention, it would have been obvious to one of ordinary skill in the art to use a hardenable, flowable polymeric material, such as a resin, to encapsulate the wires of Chiu because, in the absence of the disclosure of any particular

material, one of ordinary skill in the art would look to use a conventional material, such as a resin disclosed by Chan, to form the encapsulant.

In reference to claims 37 and 49, as can been seen in Figure 4 of Chiu, the glob-top material is inserted to extend outwardly between the edges of at least two die proximate each side of the through-slots.

In reference to claims 39 and 51, Chiu discloses encapsulating the wires but not the semiconductor dice (Fig. 4; col. 2, ln. 31-32). Chan's IC package has both the semiconductor dice and the wires encapsulated to hermetically protect them from moisture (Fig. 1 and 5, col. 6, ln. 54-58; col. 7, ln. 33-35). At the time of the invention, it would have been obvious to one of ordinary skill in the art to encapsulate the dice of Chiu in addition to the wires because, as is well known in the art, semiconductor dice can be fatally damaged by moisture, and by hermetically encapsulating them, the dice can be protected against malfunction.

Response to Arguments

Applicant's arguments filed October 8, 2002 have been fully considered but they are not persuasive.

Applicants argue that the rejection of claims 32-37, 39, 44-49 and 51 as being unpatentable over Chan et al. (US 5,998,860) in view of Lin et al. (US 5,239,198) is improper because Chan allegedly teaches that the SIMM of his invention is not to be permanently connected to a motherboard but instead is made so as to fit into an expansion slot. However, what Chan actually teaches is that his invention (attaching chips to both sides of a PCB) is applicable to a variety of integrated circuit modules. For example, Chan states, "While the making and using of various embodiments of the present invention are discussed in detail

below, it should be appreciated that the present invention provides many applicable inventive concepts which can be embodied in a wide variety of specific contexts. The specific embodiments discussed herein are merely illustrative of specific ways to make and use the invention and do not delimit the scope of the invention. The present invention is related to high frequency integrated circuit design for making a double sided SIMM. The double sided SIMM uses a double sided substrate to achieve high speed performance and to meet the space constraint requirements of modern semiconductors." (col. 2, ln. 63-col. 3, ln. 3). Chan then goes on to state, "It should be understood by one skilled in the art that the terms 'topa' [sic] and 'bottom' as well as the terms 'side' and 'end' are used for illustration purposes only, as the double sided SIMM 20 of the present invention can be assembled and used in a variety of positions and ways." (col. 4, ln. 46-51). From these statements, it is clear that Chan does not intend his invention to be limited to the one embodiment shown in the drawings (a SIMM that is to be attached to an expansion slot). Applicant argues that the Chan reference teaches away from modifying it as suggested by Lin. However, as is discussed above, Chan does not limit his invention to non-permanently attaching to an expansion slot but actually states that one of ordinary skill in the art can modify his double-sided SIMM invention to be "assembled and used in a variety of positions and ways."

Applicants argue, "There is no motivation or suggestion in Lin et al. to modify its disclosure to use the BOC type of mounting taught by Chan et al." However, none of the rejections in the previous Office Action, nor this Office Action, suggest modifying the Lin reference to incorporate the type of mounting taught by Chan. Therefore, this argument is moot.

In reference to the rejection of claims 32, 38, 44 and 50 as being unpatentable over Chiu (US 5,243,497) in view of Lin et al., Applicants argue that there is no suggestion or motivation to modify Chiu using the connection method of Lin because "Chiu is silent as to the method that it can be connected to higher level assemblies." However, as presented above and in the Office Action mailed July 2, 2002, the motivation to combine the Chiu and Lin references involves two factors. Firstly, as stated by Applicants, Chiu does not state what type of connection is to be used to connect the integrated circuit module to higher level assemblies, even though it is inherent that some type of connection to higher assemblies must be formed on the module. Secondly, Lin states that the solder-ball type of connection of his invention can be used to successfully mount an integrated circuit module regardless of whether the module is mounted vertically or horizontally to higher level assemblies. One of ordinary skill in the art would have found it obvious to apply the solder-ball connection of Lin to the module of Chiu because Chiu does not disclose any connection method while Lin teaches that solder-ball connection can be used successfully to mount the module regardless of the modules orientation.

Applicants argue, "There is no motivation or suggestion in Lin et al. to modify its disclosure to use the BOC type of mounting taught by Chiu" However, none of the rejections in the previous Office Action, nor this Office Action, suggest modifying the Lin reference to incorporate the type of mounting taught by Chiu. Therefore, this argument is moot.

The rejections made in the Office Action mailed July 2, 2002 are maintained.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christy L. Novacek whose telephone number is (703) 308-5840. The examiner can normally be reached on Monday-Thursday and alternate Fridays 7:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (703) 308-4905. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

CLN
March 13, 2003

AMIR ZARABIAN
SUPERVISORY PATENT EXAMINER
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